UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,233	11/19/2001	Yvon Gris	S1022/8800	8198

23628 7590 02/20/2004

WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,233	GRIS ET AL.	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-15,20-37,39-42 and 45-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-15,20-37,39-42 and 45-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Transitional After Final Practice

1. Since this application is eligible for the transitional procedure of 37 CFR 1.129(a), and the fee set forth in 37 CFR 1.17(r) has been timely paid, the finality of the previous Office action is hereby withdrawn pursuant to 37 CFR 1.129(a). Applicant's first submission after final filed on 1/26/2004 has been entered.

Terminal Disclaimer

2. The terminal disclaimer filed on 1/26/2004 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US 6,165,265 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 11-15, 20-37, 39-42 and 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US 5,028,556) in view of Sugano et al (US 4,469,527) and Meyerson (US 5,298,452).

Chang discloses a substrate **11** comprising silicon is masked and implanted with P+ ions, such as positively charged boron ions, to form a buried layer **13** and silicon is epitaxially grown on top of the substrate and the buried layer and heating the substrate to a predetermined temperature to form wells therein (col 2, ln 35-68 and claim 1). Chang discloses implanting ions into a substrate, as applicant, this inherently causes defects.

Chang does not teach forming defects in a region of a substrate by implanting electrically neutral species.

In a method of making a semiconductor device, note entire reference, Sugano et al teaches a silicon substrate having a silicon oxide film on the surface thereon is irradiated with thermal neutron beams, this reads on applicant's implanting electrically neutral species, so that lattice defects were produced throughout the silicon substrate to make it semi-insulating and removing the silicon oxide film (col 11, ln 65 to col 12, ln 15). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Chang with Sugano et al's thermal neutron irradiation to facilitate spatially homogeneous introduction of a desired amount phosphorous therein (col 4, ln 45-65) and reduce capacitance (col 2, ln 15-67).

The combination of Chang and Sugano et al is silent to depositing a silicon layer on the region at a temperature of less than 750°C.

Meyerson teaches a method of forming epitaxial silicon using silane and a hydrogen carrier gas at a growth temperature of less than 800°C at a pressure of 10^{-2} to 10^{-4} Torr (1.3 to 0.013 Pa). Meyerson also teaches excellent uniformity is obtained across the wafer because of the low pressure and forming a (col 9, ln 9-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Chang and Sugano et al with Meyerson process of forming epitaxial silicon at reduced temperatures to form an epitaxial silicon layer with excellent uniformity at reduced operating temperatures.

Referring to claim 12, the combination of Chang, Sugano et al and Meyerson teach heat treating after epitaxially growing a material on the buried region (Chang claim 1).

Referring to claims 13-15 and 34-37, the combination of Chang, Sugano et al and Meyerson teaches silane and hydrogen at a pressure of 1.3 Pa.

Referring to claim 22, the combination of Chang, Sugano et al and Meyerson teaches implanting boron ions.

Referring to claims 20, the combination of Chang and Meyerson does not teach implanting with fluorine atoms. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination Chang and Meyerson by using a fluorine dopant because a fluorine dopant is well known in the art.

Referring to claim 21, 24 39, and 41, the combination of Chang, Sugano et al and Meyerson teaches removing an oxide layer.

Referring to claim 29, the combination of Chang, Sugano et al and Meyerson is silent to the crystallinity of the substrate. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Chang, Sugano et al and Meyerson by using a single crystalline substrate because single crystalline substrates have improved conductivity characteristics over amorphous substrates.

Referring to claims 27 and 32, the combination of Chang, Sugano et al and Meyerson is silent to the silicon layer is deposited with a different orientation than that of the substrate. However, since the combination of Chang, Sugano et al and Meyerson teaches the method claimed, under the principle of inherency the invention is considered to be anticipated by the combination of Chang, Sugano et al and Meyerson.

Referring to claims 23 and 40, the combination of Chang, Sugano et al and Meyerson does not teach the density of interstitial defects. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Chang, Sugano et al and Meyerson by conducting routine experimentation to determine the optimum amount of interstitial defects per one hundred silicon atoms.

5. Claims 11-15, 20-37, 39-42 and 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US 5,028,556) in view of Sugano et al (US 4,469,527) and Agnello et al (5,378,651).

The combination of Chang and Sugano et al teach all of the limitations of claim 11, as discussed previously, except depositing silicon at a temperature of less than 750°C.

In a method of depositing silicon, note entire reference, Angello et al teaches an ultra-clean deposition process and the highest pressure available is 1 atmosphere (101325 Pa). Angello et al also teaches a deposition temperature of 550°C-850°C and deposition of single crystalline silicon in single crystal regions and polycrystalline silicon in insulator areas (col 6, ln 1-50).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Chang and Sugano et al with Angello's process of forming epitaxial silicon at reduced temperatures at reduced operating temperatures, which reduces operating costs.

Referring to claim 11, the combination of Chang, Sugano et al and Angello et al teach a temperture of 550-850°C. Overlapping ranges are held to be obvious (MPEP 2144.05). Furthermore, a lower temperature would be desirable because a lower temperature would reduce operating costs; therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Chang, Sugano et al and Angello et al by optimizing the temperature to obtain same by conducting routine experimentation of a result effective variable.

Referring to claim 45-46, the combination of Chang, Sugano et al and Angello et al teach pressure up to 1 atmosphere (101325 Pa). Overlapping ranges are held to be obvious (MPEP 2144.05). Furthermore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Chang, Sugano et al and Angello et al by optimizing the pressure to obtain same by conducting routine experimentation of a result effective variable.

6. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US 5,028,556) in view of Sugano et al (US 4,469,527) and Meyerson (US 5,298,452) or in view of Sugano et al (US 4,469,527) and Angello et al (US 5,378,651) as applied to claim 11 above, and further in view of Wu et al (US 4,584,0296).

The combination of Chang, Sugano et al and Meyerson or the combination of Chang, Sugano et al and Angello et al teach all of the limitations of claim 20, as discussed previously, except forming defects by implanting fluorine atoms.

In a method of ion implantation, note entire reference, Wu et al teaches implanting fluorine into a single crystal silicon substrate to make the surface of the substrate amorphous (col 3, ln 1-30) because fluorine decreases the temperature at which an effective level of conductivity is achieved (Example 1). Wu et al teaches wafer receiving both fluorine and phosphorous implants reached an effective level of conductivity at a lower temperature than implanting only with phosphorous (col 4, ln 30-57). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Chang, Sugano et al and Meyerson or the combination of Chang, Sugano et al and Angello et al with Wu et al's fluorine implantation to reduce the temperature required to reach an effective level of conductivity (col 4, ln 50-57).

Response to Arguments

7. Applicant's arguments with respect to claims 11-15, 20-37, 39-42 and 45-48 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Plumton (US 5,554,561) teaches that doping by implantation affects the crystal orientation of GaAs grown on GaAs (col 1, ln 60-67 and col 7, 50-67).

Kagata et al (US 5,221,412) teaches growing a single crystal Si film on a Si single crystal substrate at 700°C or lower at a normal or reduced pressure of about 50 Torr (col 3, ln 10-65).

Burns et al (US 5,011,789) teaches growing a single crystal Si film at 650-800°C at a pressure of 6 Pa and the importance of low temperatures to prevent transfer of dopants (col 3, ln 35 to col 4, ln 15 and col 6, ln 1-5).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1765

MJS

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER